Impact of Proton Irradiation on the RF Performance of 0.12 μm CMOS Technology

Sunitha Venkataraman, Becca M. Haugerud, Enhai Zhao, Bhaskar Banerjee, Akil Sutton, Paul W. Marshall*, Chang-Ho Lee, John D. Cressler, Joy Laskar, John Papapolymerou and Alvin J. Joseph**

School of Electrical and Computer Engineering and Georgia Electronic Design Center,
85 5$^{\text{th}}$ Street, NW, Georgia Institute of Technology, Atlanta, GA 30332 USA. / Email: sunitha@ece.gatech.edu
*Consultant to NASA-GSFC, **IBM Microelectronics, Essex Junction, VT 05452, USA.

Abstract— **The effects of 63 MeV proton irradiation on the *dc* and *RF* performance of a 0.12 μm CMOS technology is presented for the first time. The radiation response of the CMOS devices was investigated up to an equivalent total gamma dose of 1.0 Mrad(Si). Measurements of the *dc* current-voltage, low-frequency $(1/f)$ noise, S-parameters, and broadband noise characteristics of the devices were performed before and after irradiation at room temperature. These scaled CMOS devices show a very slight degradation of threshold voltage, transconductance (g_m), and $1/f$ noise after proton irradiation without any intentional radiation hardening. High-frequency measurements on the irradiated devices show that there is very little or no perceptible degradation of S-parameters, cut-off frequency (f_T), or broadband noise characteristics to 1 Mrad(Si) exposure levels. These results suggest that this 0.12 μm CMOS technology is well-suited for the development of total-dose radiation tolerant analog and RF circuits without additional radiation hardening.**

I. MOTIVATION

Aggressive scaling into the deep sub-micron regime has enhanced the frequency response and noise performance of standard Si CMOS devices. This performance improvement, coupled with its high-density integration capability, cost effectiveness, and manufacturing maturity makes CMOS technology attractive for integrating RF front-ends and the base-band analog and digital circuitry onto a single chip. Down-scaling of CMOS devices also natually requires thinner gate oxides, which is known to have a significant positive impact on CMOS device performance in an ionizing radiation environment since thin, high quality gate oxides exhibit reduced sensitivity to total dose radiation effects. The superior radiation response of aggressively scaled CMOS technologies can thus be potentially harnessed in the development of radiation tolerant electronic systems. Applications of radiation-tolerant CMOS integrated circuits include satellite systems, space missions, imaging and high energy physics detectors. The effects of ionizing radiation on the *dc*, low-frequency noise, and small-signal performance of CMOS devices have been previously reported [1] - [4].

In this paper, we present for the first time proton radiation effects on the *dc*, low-frequency $(1/f)$ noise, small-signal, and *RF* noise performance of a aggressively-scaled 0.12 μm CMOS technology. Off-state leakage and radiation-induced shift of threshold voltage and transconductance are used to assess the *DC* performance of the devices. Low-frequency $(1/f)$ noise measurements were used to understand the radiation-induced oxide charge buildup. *RF* performance of the CMOS devices under proton radiation was characterized using S-parameter and broad-band noise measurements, and used to assess its capabilities for RF circuits.

II. EXPERIMENT

The MOSFETs used in this study are contained in a fully-integrated, SiGe HBT BiCMOS technology [5]. The process offers CMOS devices in 1.2V and 2.5V flavors (Lg drawn of 0.12μm and 0.24μm respectively. nFETs with a drawn W/L of 10/0.12 were selected for *dc* and low-frequency noise measurements. Multi-fingered NMOS devices were chosen for the small-signal *ac* and broadband noise characterization. For brevity, the pFETs are known to be radiation hard and are not addressed here.

The samples were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) located several meters upstream of the target establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 5 nA to 80 nA allow testing with proton equivalent gamma doses from 10 krad to 1 Mrad. The dosimetry system has been previously described [6], [7], and is accurate to about 10%. At a proton fluence of 1×10^{12} p/cm^2, the measured equivalent gamma dose was approximately 135 krad(Si). The 0.12μm Si nFETs were irradiated with the gate terminal biased at V_{DD} (1.2V) and the drain, source, and substrate terminals grounded for the DC measurements (i.e. worst case conidtions), and with all terminals floating for the *ac* measurements, at doses ranging from 1 krad to 1 Mrad. Samples for *dc* measurements were mounted in 24 pin DIP packages and were wire-bonded. The *ac* samples were mounted on ceramic holders and exposed to proton radiation up to 1 Mrad(Si) equivalent gamma dose.

The *dc* device characterization was performed using a HP 4155C Semiconductor Parameter Analyzer. The low-frequency
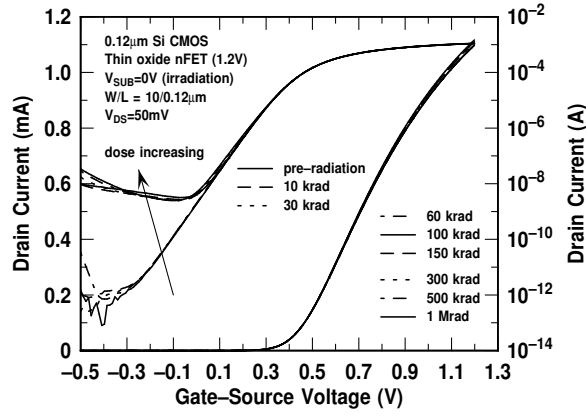
Fig. 1. Drain current as a function of gate-to-source voltage, before and after radiation for an nFET with W/L = 10.0/0.12
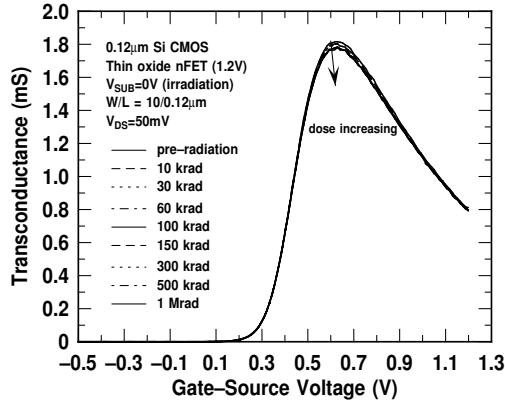

Fig. 3. The threshold voltage shift as a function of equivalent total dose for both the 10.0/0.12 nFETs

Fig. 2. Transconductance (g_m) as a function of drain current, before and after radiation for an nFET with W/L = 10.0/0.12

noise measurements were performed using a HP 3562 dual channel dynamic signal analyzer [8]. S-Parameters of the test devices and their corresponding "Open" and "Short" de-embedding structures were measured using a HP 8510C VNA. The conventional "Open-Short" de-embedding technique was performed on the raw S-parameters of the devices to elimi-nate the effects of pad parasitics. The high-frequency noise parameters were measured from 2 GHz to 26 GHz using the ATN NP5B Noise measurement system, which employs the "multiple source impedance technique" for the extraction of noise parameters. The devices under test were biased in the saturation region from moderate to strong inversion, as this is the typical biasing condition encountered in most analog and RF circuits. All the measurements were performed at room temperature before and after the devices were exposed to proton radiation.

III. RESULTS AND DISCUSSION

A. dc Performance

The pre- and post-radiation drain current (I_D) versus gate-to-source voltage (V_{GS}) for the $10\mu m/0.12\mu m$ nFET is shown in Fig. 1. The drain current is plotted on both linear and logarithmic scales. The sub-threshold characteristics indicate
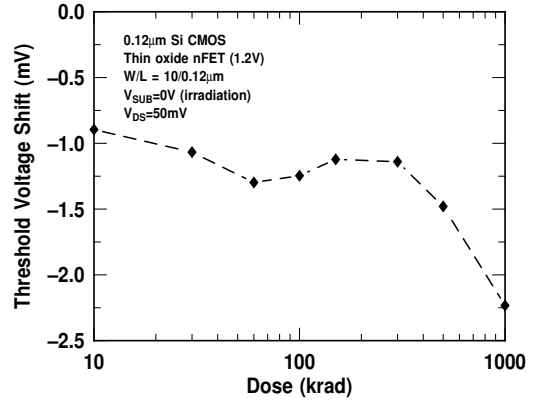
that the off-state leakage current increases from about 1 pA before radiation to about 50 nA after a total dose of 1 Mrad. This off-state leakage is attributed to the device region where the poly-silicon gate overlaps the shallow trench isolation, where a parasitic inversion channel is produced at sufficiently high radiation damage. We observe that at equivalent doses higher than 150 krad, the gate bias has no control over the leakage current for $V_{GS} < 0V$ as the parasitic conduction deep in the bulk dominates over the parasitic conduction at the surface of the shallow trench isolation (STI) corner [9]. However, this level of parasitic leakage is significantly better than that observed in 0.18um CMOS technology, and is attributed to the thinner shallow trench used in the present technology.

The linear I_D versus V_{GS} curve shows that there is almost no perceptible degradation in the drain current in the strong inversion region of operation. As seen in Fig. 2, the radiation induced transconductance degradation is almost negligible. Fig. 3 shows that the maximum radiation induced threshold voltage shift (ΔV_{th}) for the 10/0.12 nFETs is about $-2.2mV$ at 1 Mrad total dose. As expected, the 0.12 μm nFETs exhibit a very slight radiation-induced dc performance degradation, since the devices have a very thin (2.2 nm) high-quality gate oxide.

B. Low-frequency ($1/f$) Noise Performance

Low-frequency ($1/f$) noise in MOSFETs is highly sensitive to the defects present at or near the Si/SiO_2 interface. Oxide-trap charges are mainly responsible for the observed $1/f$ noise in MOSFETs. The drain current noise spectral density is often modeled by the empirical relation:

$$S_{Id} = \frac{K \ g_m^2}{C_{OX}^2 WLf} \tag{1}$$

where, K is a process-dependent parameter for $1/f$ noise and C_{OX} is the gate oxide capacitance per unit area.

On-wafer $1/f$ noise measurements were performed on the nFETs with W/L of 10/0.12, before and after radiation (at an equivalent total dose of 1 Mrad). The devices were biased in the saturation region (V_{GS}=1.0V, V_{DS}=1.5V) for relevance
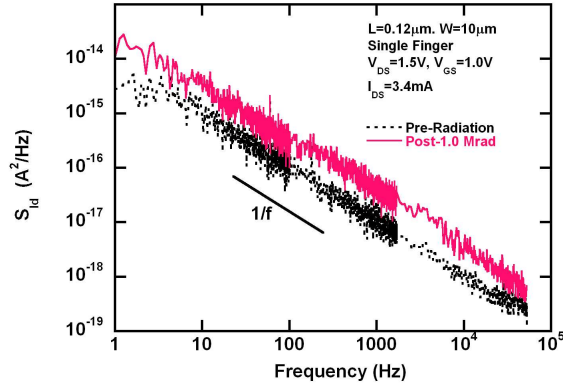
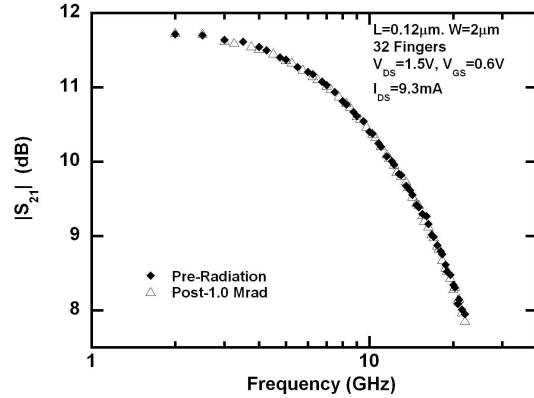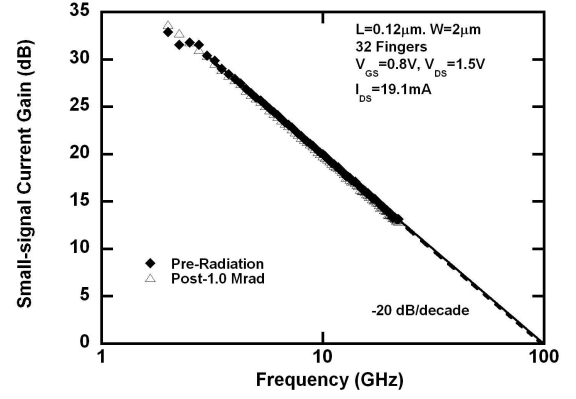Fig. 4. Drain noise current spectrum, before and after irradiation, for an nFET with W/L = 10.0/0.12

Fig. 6. Small-signal current gain h_{21} as a function of frequency, before and after irradiation, for an nFET with W/L = 2.0/0.12 and 32 gate fingers.
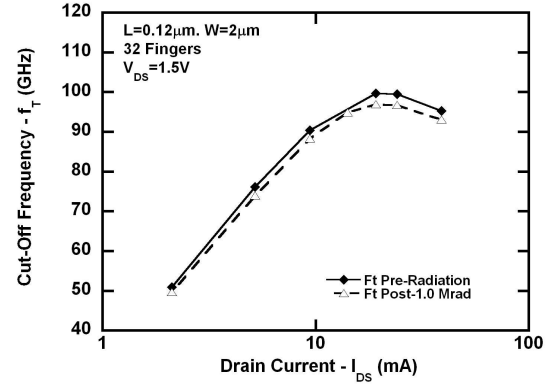

Fig. 5. Magnitude of S_{21} as a function of frequency, before and after irradiation, for an NFET with W/L = 2.0/0.12 and 32 gate fingers.

Fig. 7. Cut-off frequency f_T as a function of drain current, before and after irradiation, for an nFET with W/L = 2.0/0.12 and 32 gate fingers.

to circuit design. The drain current noise spectral density (S_{Id}) measured before and after irradiation is shown in Fig. 4. A slight increase in $1/f$ noise is observed after radiation, which is mainly due to the radiation-induced increase of oxide-trapped charges [1], [10]. The results indicate that these aggressively scaled $0.12\mu m$ nFETs are less sensitive to radiation-induced $1/f$ noise degradation because of the very thin (2.2nm in this case) and high quality gate oxide.

C. Small-Signal Performance

On-wafer S-Parameter measurements were performed on an nFET with 32 gate fingers, each with a unit width of $2.0\mu m$ and length of $0.12\mu m$. Such a device geometry is of sufficient size to be useful for RF circuit applications. The raw S-parameters were de-embedded using the corresponding "Open" and "Short" structures. Fig. 5 shows a very small decrease in the magnitude of S_{21} after radiation. The cut-off frequency (f_T) can extracted from the de-embedded S-parameters and is given by the following relation:

$$f_T = \frac{g_m}{2\pi \ (C_{gs} + C_{gd})} \qquad (2)$$

Fig. 6 shows the measured small-signal current gain (h_{21}) as a function of frequency at peak f_T for a 2.0/0.12 (32 finger)

nFET. A near 20dB/decade slope is obtained across a wide frequency range both before and after radiation. The cut-off frequency versus drain current characteristics, before and after radiation, is shown in Fig. 7. The small decrease in f_T after radiation is due to the slight degradation of g_m (2). We see that the peak f_T for the 2/0.12 (32 finger) nFETs is 100 GHz prior to radiation and is 97 GHz after 1 Mrad total dose, thus exhibiting a negligible radiation-induced change in the overall frequency response.

D. Broadband Noise Performance

The main sources of broadband noise in MOSFETs are the channel thermal noise, gate resistance-induced thermal noise, and the induced gate noise. The minimum noise figure can be described using Fukui's equation [11]:

$$F_{min} = 1 \ + \ K \ \frac{f}{f_T} \ \sqrt{g_m(R_g + R_s)} \qquad (3)$$

where, f is the frequency of operation, R_g and R_s are the gate and source resistances and K is a technology-dependent fitting parameter.

Using (2), F_{min} can be expressed as

$$F_{min} = 1 \ + \ K \ \frac{f \ 2\pi(C_{gs} + C_{gd})}{\sqrt{g_m}} \ \sqrt{R_g + R_s} \qquad (4)$$
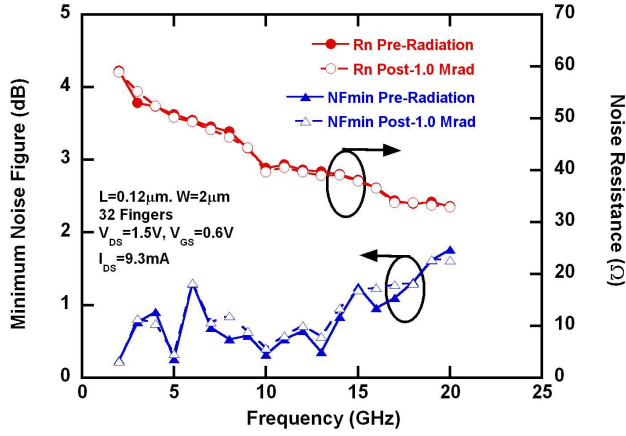
Fig. 8. Minimum Noise Figure and Noise Resistance as a function of frequency, before and after radiation, for a NMOS device with W/L = 2.0/0.12 and 32 fingers

Fig. 10. Associated gain versus frequency, before and after radiation, for an nFET device with W/L = 2.0/0.12 and 32 gate fingers.
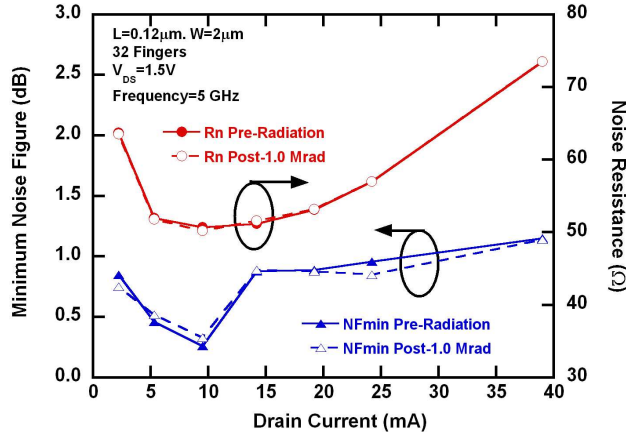

Fig. 9. Minimum Noise Figure and Noise Resistance at 5 GHz as a function of drain current, before and after irradiation, for an nFET with W/L = 2.0/0.12 and 32 gate fingers.

From (4), one would expect a higher F_{min} after irradiation, due to the slight decrease in g_m.

Fig. 8 and 9 show the minimum noise figure and noise resistance as a function of frequency and drain current, before and after radiation, for an nFET with 32 gate fingers, each with a W/L of 2/0.12. We observe a very slight degradation of F_{min}, as expected, and almost no change in the noise resistance after radiation. The associated gain of the device also remains unchanged after irradiation, as shown in Fig. 10.

IV. SUMMARY

The effects of proton radiation on the *dc*, low-frequency $1/f$ noise, small-signal, and *RF* noise performance of a 0.12 μm CMOS technology is presented for the first time. The radiation response of nFETs was studied up to an equivalent gamma dose of 1 Mrad (Si). The nFETs show a very slight degradation of threshold voltage and transconductance up to 1 Mrad. The thin and high quality gate oxide used in these devices also lead to only a small degradation of low
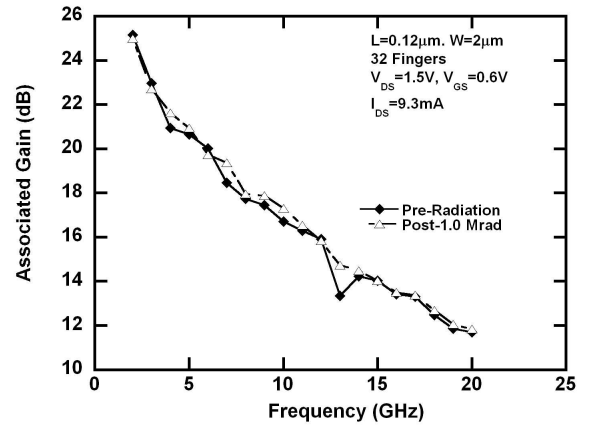
frequency $1/f$ noise after proton exposure. The small-signal gain and cut-off frequency (f_T) show a very small decrease after irradiation up to 1 Mrad(Si). There is no perceptible change in the *RF* noise characteristics of the nFETs after proton radiation. The results indicate that this 0.12 μm CMOS technology exhibits reduced sensitivity to ionizing radiation compared to the previous-generation CMOS technologies, and thus aggressive scaling has a favorable impact on total dose radiation tolerance, suggesting that it is well-suited for RF and circuit applications in radiation environments.

REFERENCES

[1] D. M. Fleetwood *et al.*, *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1953-1964, 1994.
[2] Y. Li *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1834-1838, 2003.
[3] E. Simoen *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2426-2432, 2003.
[4] Y. Li *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1827-1833, 2003.
[5] B. A. Orner *et al.*, *Proce 2003 BCTM*, pp. 203-206, 2003.
[6] K. M. Murray *et al.*, *Nuclear Inst. and Methods*, vol. B56/57, p. 616, 1991.
[7] P. W. Marshall *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1958-1965, 1994.
[8] E. Zhao *et al*, *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2230-2236, 2002.
[9] G. Niu *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1841-1847, 1999.
[10] T. L. Meisenheimer *et al.*, *IEEE Trans. Nucl. Sci.*, vol. 38, no. 6, pp. 1297-1303, 1991.
[11] H. Fukui *et al*, *IEEE Trans. Electron Devices*, vol. 26, pp. 1032-1037, 1979.